ABSTRACT OF THE DISCLOSURE

An apparatus and method in a pipelined microprocessor for replacing one of two target addresses in a branch target address cache (BTAC) line. If only one of the two entries is invalid, the invalid entry is replaced. If both entries are valid, the least recently used entry is replaced. If both entries are invalid, the entry is replaced corresponding to the side of the BTAC, indicated by a global status register, not last written to with an invalid entry. In one embodiment, the global status is updated only if a side is written when both entries are invalid. In another embodiment, the BTAC stores N entries per line, where N is greater than 1. The status register maintains information for determining which of the N sides is least recently written. The least recently written side is chosen for replacement.